CLAIMS

1. A computer system comprising:

at least one processor;

a controller for coupling said at least one processor to a peripheral bus control block and a memory module bus;

at least one peripheral bus slot coupled to said peripheral bus control block by a peripheral bus;

at least one memory module slot coupled to said memory module bus; and

a processor element associated with said at least one memory module slot for providing a data connection to an external device coupled thereto.

2. The computer system of claim 1 further comprising:

a control connection to said processor element coupled to said peripheral bus for indicating to said at least one processor an arrival of data on said data connection to said processor element.

3. The computer system of claim 1 wherein said memory module bus comprises a DIMM bus.

4. The computer system of claim 3 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.

5. The computer system of claim 1 wherein said memory module bus comprises a RIMM bus.

6. The computer system of claim 5 wherein said processor element comprises a RIMM physical format for retention within said at least one memory module slot.

7. The computer system of claim 1 wherein said external device comprises one of another computer system, switch or network.

8. The computer system of claim 1 wherein said peripheral bus comprises a PCI bus.

9. The computer system of claim 1 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.

10. The computer system of claim 1 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.

11. The computer system of claim 1 wherein said processor element comprises:

a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.

12. The computer system of claim 1 wherein said at least one processor comprises a plurality of processors.

13. A computer system comprising:

at least one processor;

a controller for coupling said at least one processor to a graphics control block and a memory module bus;

at least one graphics bus connection coupled to said graphics control block by a graphics bus;

at least one memory module slot coupled to said memory module bus; and

a processor element associated with said at least one memory module slot for providing a data connection to an external device coupled thereto.

14. The computer system of claim 13 further comprising:

a control connection to said processor element coupled to said graphics bus for indicating to said at least one processor an arrival of data on said data connection to said processor element.

15. The computer system of claim 13 wherein said memory module bus comprises a DIMM bus.

16. The computer system of claim 15 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.

17. The computer system of claim 13 wherein said memory module bus comprises a RIMM bus.

18. The computer system of claim 17 wherein said processor element comprises a RIMM physical format for retention within said at least one memory module slot.

19. The computer system of claim 13 wherein said external device comprises one of another computer system, switch or network.

20. The computer system of claim 13 wherein said peripheral bus comprises an AGP bus.

21. The computer system of claim 13 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.

22. The computer system of claim 13 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.

23. The computer system of claim 13 wherein said processor element comprises:

a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.

24. The computer system of claim 13 wherein said at least one processor comprises a plurality of processors.

25. A computer system comprising:

at least one processor;

a controller for coupling said at least one processor to a system maintenance control block and a memory module bus;

at least one system maintenance bus connection coupled to said system maintenance control block by a system maintenance bus;

at least one memory module slot coupled to said memory module bus; and

a processor element associated with said at least one memory module slot for providing a data connection to an external device coupled thereto.

26. The computer system of claim 25 further comprising:

a control connection to said processor element coupled to said system maintenance bus for indicating to said at least one processor an arrival of data on said data connection to said processor element.

27. The computer system of claim 25 wherein said memory module bus comprises a DIMM bus.

28. The computer system of claim 27 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.

29. The computer system of claim 25 wherein said memory module bus comprises a RIMM bus.

30. The computer system of claim 29 wherein said processor element comprises a RIMM physical format for retention within said at least one memory module slot.

31. The computer system of claim 25 wherein said external device comprises one of another computer system, switch or network.

32. The computer system of claim 25 wherein said peripheral bus comprises an SM bus.

33. The computer system of claim 25 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.

34. The computer system of claim 25 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.

35. The computer system of claim 25 wherein said processor element comprises:

a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.

36. The computer system of claim 25 wherein said at least one processor comprises a plurality of processors.

37. A processor element for a memory module bus of a computer system, said processor element comprising:

a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto and operative to alter data provided thereto on said memory module bus; and

a data connection coupled to said field programmable gate array for providing said altered data to an external device coupled thereto.

38. The processor element of claim 37 further comprising:

a control connection coupled to said processor element for indicating to a processor of said computer system an arrival of data on said data connection from said external device.

39. The processor element of claim 38 wherein said control connection indicates said arrival of data to said processor by means of a peripheral bus.

40. The processor element of claim 39 wherein said peripheral bus comprises a PCI bus.

41. The processor element of claim 38 wherein said control connection indicates said arrival of data to said processor by means of a graphics bus.

42. The processor element of claim 41 wherein said graphics bus comprises an AGP bus.

43. The processor element of claim 38 wherein said control connection indicates said arrival of data to said processor by means of a system maintenance bus.

44. The processor element of claim 43 wherein said graphics bus comprises an SM bus.

45. The processor element of claim 37 wherein said memory module bus comprises a DIMM bus.

46. The processor element of claim 45 wherein said processor element comprises a DIMM physical format.

47. The processor element of claim 37 wherein said memory module bus comprises a RIMM bus.

48. The processor element of claim 47 wherein said processor element comprises a RIMM physical format.

49. The processor element of claim 37 wherein said external device comprises one of another computer system, switch or network.

50. The processor element of claim 37 wherein said processor of said computer system comprises a plurality of processors.

51. The processor element of claim 37 wherein said field programmable gate array is further operative to alter data provided thereto from said external device on said data connection and providing said altered data on said memory module bus.